

I Claim:

- 1 1. A current mode pipeline analog-to-digital converter apparatus including a plurality of stages; each respective stage of said plurality of stages comprising:
 - 3 (a) a respective residue amplifier including a first amplifying unit and a second amplifying unit; each of said first and second amplifying units having an inverting input locus, a non-inverting input locus and an output locus; each of said first and second amplifying units receiving a differential input data signal at one input locus of said inverting input locus and said non-inverting input locus; the other input loci of said first and second amplifying units than said one input locus receiving a first current signal in a first current direction providing a DC level setting signal for each of said first and second amplifying units; signals presented at said output loci substantially representing said input data signal less said DC level setting signal; and
 - 13 (b) a counter-current signal generating unit coupled with said other input loci at a single coupling locus; said counter-current signal generating unit presenting a second current signal in a second current direction opposite to said first current direction providing a DC level control signal for each of said first and second amplifying units.
- 1 2. A current mode pipeline analog-to-digital converter apparatus including a plurality of stages as recited in Claim 1 wherein said first current signal is provided by an NPN digital-to-analog converter unit.
- 1 3. A current mode pipeline analog-to-digital converter apparatus including a plurality of stages as recited in Claim 1 wherein said counter-current signal generating unit is a PNP digital-to-analog converter unit.
- 1 4. A current mode pipeline analog-to-digital converter apparatus including a plurality of stages as recited in Claim 2 wherein said counter-current signal generating unit is a PNP digital-to-analog converter unit.

1 5. An analog-to-digital converter apparatus having a plurality of stages; each respective
2 stage of said plurality of stages comprising:
3 (a) a residue amplifier having a first amplifier unit and a second amplifier unit;
4 each of said first amplifier unit and said second amplifier unit having a first input
5 locus, a second input locus and an output locus; said first and second amplifier
6 units cooperating in receiving a differential input data signal at said first input loci
7 of said first and second amplifier units;
8 (b) a DC level setting signal unit coupled with said second input loci of said first
9 and second amplifier units; said DC level setting signal unit providing a DC level
10 setting current in a first current direction to said second input loci; and
11 (c) a counter-current signal generating unit coupled with said second input loci via
12 a single coupling locus common with said second input loci; said counter-current
13 signal generating unit providing a control current signal to said second input loci
14 in a second current direction opposite to said first current direction; said control
15 current signal providing a DC level control for each of said first and second
16 amplifier units.

1 6. An analog-to-digital converter apparatus having a plurality of stages as recited in
2 Claim 5 wherein said DC level setting current unit is an NPN digital-to-analog
3 converter unit.

1 7. An analog-to-digital converter apparatus having a plurality of stages as recited in
2 Claim 5 wherein said counter-current signal generating unit is a PNP digital-to-analog
3 converter unit.

1 8. An analog-to-digital converter apparatus having a plurality of stages as recited in
2 Claim 6 wherein said counter-current signal generating unit is a PNP digital-to-analog
3 converter unit.

1 9. A method for reducing noise in input signals to a residue amplifier in an analog-to-
2 digital converter apparatus; the residue amplifier having a first amplifier unit and a
3 second amplifier unit; each of said first amplifier unit and said second amplifier unit
4 having a first input locus, a second input locus and an output locus; said first and
5 second amplifier units cooperating in receiving a differential input data signal at said
6 first input loci of said first and second amplifier units; a DC level setting signal unit
7 coupled with said second input loci of said first and second amplifier units provides a
8 DC level setting current in a first current direction to said second input loci; the
9 method comprising the steps of :

10 (a) providing a counter-current signal generating unit coupled with said second
11 input loci via a single coupling locus common with said second input loci; and
12 (b) operating said counter-current signal generating unit to provide a control
13 current signal to said second input loci in a second current direction opposite to
14 said first current direction to establish a DC level control for each of said first and
15 second amplifier units.

1 10. A method for reducing noise in input signals to a residue amplifier in an analog-to-
2 digital converter apparatus as recited in Claim 9 wherein said DC level setting unit is
3 an NPN digital-to-analog converter unit.

1 11. A method for reducing noise in input signals to a residue amplifier in an analog-to-
2 digital converter apparatus as recited in Claim 9 wherein said counter-current signal
3 generating unit is a PNP digital-to-analog converter unit.

1 12. A method for reducing noise in input signals to a residue amplifier in an analog-to-
2 digital converter apparatus as recited in Claim 10 wherein said counter-current signal
3 generating unit is a PNP digital-to-analog converter unit.